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			BAISA, JOSELITO SASIS	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Application No. Applicant(s) 10/538,221 BURKE ET AL. Office Action Summary Examiner Art Unit JOSELITO BAISA 2832 -- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --Period for Reply A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS. WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION. Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication. If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b). Status 1) Responsive to communication(s) filed on 15 January 2008. 2a) This action is FINAL. 2b) This action is non-final. 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11, 453 O.G. 213. Disposition of Claims 4)\ Claim(s) 16-28.32.33.43.47-49.54-66.70.71 and 73-76 is/are pending in the application. 4a) Of the above claim(s) is/are withdrawn from consideration. 5) Claim(s) _____ is/are allowed. 6) Claim(s) 16-28,32,33,43,47-49,54-66,70,71 and 73-76 is/are rejected. 7) Claim(s) _____ is/are objected to. 8) Claim(s) _____ are subject to restriction and/or election requirement. Application Papers 9) The specification is objected to by the Examiner. 10) The drawing(s) filed on 15 January 2008 is/are: a) accepted or b) objected to by the Examiner. Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a). Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d). 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152. Priority under 35 U.S.C. § 119 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f). a) All b) Some * c) None of: Certified copies of the priority documents have been received. 2. Certified copies of the priority documents have been received in Application No. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)). * See the attached detailed Office action for a list of the certified copies not received. Attachment(s) 1) Notice of References Cited (PTO-892) 4) Interview Summary (PTO-413) Paper Ne(s)/Vail Date ____

Notice of Draftsparson's Patent Drawing Review (PTO-946)

 Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _

5) Notice of Informal Patent Application

6) Other:

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DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

Claims 16-19, 32 and 33 are rejected under 35 U.S.C. 102(a) as being anticipated by Yoneda et al. [4912450].

Yoneda discloses a first metal layer 2a,

a second metal layer 2b

at least one layer of device material 1 sandwiched between the first metal layer 2a and the second metal layer 2b which function as electrodes for the device material 1.

a first terminal 4a for providing a first electrical connection to the device 1,

a second terminal 4b for providing a second electrical connection to the device 1, wherein the first terminal 4a is electrically connected to the first metal layer 2a and the second terminal 4b is insulated from the first metal layer 2a and electrically connected to the second metal layer 2b by a conductive channel 5b which passes through and is insulated from the first metal layer 2a and the layer of device material 1 and a conductive element (conductive material) that connects the conductive channel 5b to the second metal layer 2b; whereby the first terminal 4a is electrically connected to the layer of device material 1 only through the first metal layer 2a, and the second terminal 4b is electrically connected to the layer of device 1 only through the second metal layer 2b [Col. 4, Lines 31-59, Figure 1].

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Regarding claim 17, Yoneda discloses the conductive channel (5a, 5b) comprises a metal coated channel [Col. 5, Lines 1-5].

Regarding claim 18, Yoneda discloses the second terminal 4b is insulated from the first metal layer 2a by a first layer of insulating material (3a, 3b) [Col. 4, Lines 40-45, Figure 1].

Regarding claim 19, Yoneda discloses the first layer of insulating material 3a substantially covers first layer of metal 2a [Col. 4, Lines 31-39, Figure 1].

Regarding claim 32, Yoneda discloses at least one layer of device material comprises alternating layers of device material 1 and metal (2a, 2b) [Col. 4, Lines 31-41, Figure 1].

Regarding claim 33, Yoneda discloses the device is a PTC device and device material 1 is a PTC material [Col. 4, Lines 31-32].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

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Claims 20-28, 43, 47-49, 54-66, 70, 71 and 73-76 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoneda in view of Chu et al. [6377467].

Yoneda discloses the instant claimed invention discussed above except for a third layer disposed on the first layer of insulating material and the third layer is divided by an isolation area to provide the first terminal and the second terminal.

Chu discloses comprising a layer of metal (18, 16) disposed on the first layer of insulating material 14a and where the layer (18, 16) is divided by an isolation area 24a to provide the first terminal 16 and the second terminal 18 [Col. 5, Lines 8-17, Figure 1].

It would have been obvious to one having ordinary skill in the art at the time of the invention to use an isolation area separating a metal layer disposed on a surface of an insulating material as taught by Chu to the device of Yoneda.

The motivation would have been to create an insulating effect for the divided metal layer for the purpose of using the divided portions as terminals [Col. 5, Lines 12-17, Figure 1].

Regarding claims 21and 25-28, Chu discloses a third terminal 16 (lower part of device) for providing a third electrical connection to the device, a fourth terminal 18 for providing a fourth electrical connection to the device, wherein the fourth terminal 18 is electrically connected to the second metal layer 12b and the third terminal 16 is insulated from the second metal layer 12b and electrically connected to the first metal layer 12a by a second conductive channel 13 and is insulated from the second metal layer 12b; [Col. 5, Lines 3-25, Figure 1].

Chu discloses the instant claimed invention discussed above except for the second conductive channel passing through and connecting to the layer of the device material and the

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third and fourth terminals are electrically connected to the layer of device material only through first and second metal layers.

Yoneda discloses a second conductive channel 5a which passes through and is insulated from the second metal layer 2b and the layer of device material 1 and a second conductive element (conductive material on 5a) that connects the second conductive channel 5a to the first metal layer 2a; and the terminals (4a, 4b) is electrically connected to the layer of device material 1 only through the first and second metal layers (12a, 12b) [Col. 4, Lines 30-50, Figure 1].

It would have been obvious to one having ordinary skill in the art at the time of the invention to use a terminal connected electrically to the layer of device material through first and second metal layers only as taught by Yoneda to the device of Chu.

The motivation would have been for producing thermistors in minimum production steps since the resulting thermistor requires only formation of external electrode to obtain an efficient monolithic thermistor. The encapsulated thermistor also has an advantage in high or elevated temperature conditions [Col. 3, Lines 30-40].

Regarding claim 22, Yoneda discloses the conductive channel (5a, 5b) comprises a metal coated channel [Col. 5, Lines 1-5].

Regarding claim 23, Chu discloses the third terminal 16 is insulated from the second metal layer 12b by a second layer of insulating material 14b [Col. 5, Lines 3-11, Figure 1].

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Regarding claim 24, Yoneda discloses the second layer of insulating material 3b substantially covers second layer of metal 2b [Col. 4, Lines 31-40, Figure 1].

Regarding claim 55, Chu discloses a matrix (A, B) of electronic devices comprising: a first metal layer 12a, a second metal layer 12b at least one layer of device material 10 sandwiched between the first metal layer 12a and the second metal layer 12b which function as electrodes for the device material, a first array of terminals 16 for providing electrical connections to individual devices of the matrix, a second array of terminals 18 for providing electrical connections to individual devices of the matrix, herein the first array of terminals 16 are electrically connected to the first metal layer 12a and the second array of terminals 18 are insulated from the first metal layer and electrically connected to the second metal layer 12b by conductive channels 15 [Col. 5, Lines 18-22, Figures 1 and 3a].

Chu discloses the instant claimed invention discussed above except for a conductive channel passing through and is insulated from the layer of the device material and a conductive element that electrically connects the conductive channel to the second metal layer; and the first and second terminals are electrically connected to the layer of device material only through first and second metal layers only.

Yoneda discloses a conductive channel 5b which passes through and is insulated from the first metal layer 2a and the layer of device material 1 and a second conductive element (conductive material on 5b) that connects the conductive channel 5b to the second metal layer 2b; and whereby the first terminals 4a is electrically connected to the layer of device material 1

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only through the first metal layers 2a and the second terminal 4b is electrically connected to the layer of device material 1 only through second metal layer 2b) [Col. 4, Lines 30-50, Figure 1].

It would have been obvious to one having ordinary skill in the art at the time of the invention to use a terminal connected electrically to the layer of device material through first and second metal layers only as taught by Yoneda to the device of Chu.

The motivation would have been for producing thermistors in minimum production steps since the resulting thermistor requires only formation of external electrode to obtain an efficient monolithic thermistor. The encapsulated thermistor also has an advantage in high or elevated temperature conditions [Col. 3, Lines 30-40].

With respect to claims 73-76, the claims are method counterpart of structure of the rejected claim 55 and method steps therefore are inherent for manufacturing a matrix of conductive polymer device.

Regarding claim 56, Yoneda discloses the conductive channel (5a, 5b) comprises a metal coated channel [Col. 5, Lines 1-5].

Regarding claim 57, Chu discloses the second array of terminals 18 are insulated from the first metal layer 12a by a first layer of insulating material 14a [Col. 5, Lines 3-11, Figures 1 and 3a].

Regarding claim 58, Yoneda discloses the first layer of insulating material 3a substantially covers first layer of metal 2a [Col. 4, Lines 31-40, Figure 1].

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Regarding claim 59, Chu discloses a third layer of metal (16, 18) disposed on the first layer of insulating material 14a and where the third layer is divided to provide the first array of terminals 16 and the second array of terminals 18 [see Figure 3a].

Regarding claim 60, Chu discloses a third array of terminals 16 for providing electrical connections to the individual devices, a fourth array of terminals 18 for providing electrical connections to the individual devices, wherein the fourth array of terminals 18 are electrically connected to the second metal layer 12b, and the third array of terminals 16 are insulated from the second metal layer 12b and electrically connected to the first metal layer 12a by a second array of conductive channels 13 [see Figures 1 and 3a].

Chu discloses the instant claimed invention discussed above except for the second conductive channel passing through and connecting to the layer of the device material and the third and fourth terminals are electrically connected to the layer of device material only through first and second metal layers.

Yoneda discloses a second conductive channel 5a which passes through and is insulated from the second metal layer 2b and the layer of device material 1 and a second conductive element (conductive material on 5a) that connects the second conductive channel 5a to the first metal layer 2a; and the terminals (4a, 4b) is electrically connected to the layer of device material 1 only through the first and second metal layers (12a, 12b) [Col. 4, Lines 30-50, Figure 1].

It would have been obvious to one having ordinary skill in the art at the time of the invention to use a terminal connected electrically to the layer of device material through first and second metal layers only as taught by Yoneda to the device of Chu.

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The motivation would have been for producing thermistors in minimum production steps since the resulting thermistor requires only formation of external electrode to obtain an efficient monolithic thermistor. The encapsulated thermistor also has an advantage in high or elevated temperature conditions [Col. 3, Lines 30-40].

With respect to claims 73-76, the claims are method counterpart of structure of the rejected claim 60 and method steps therefore are inherent for manufacturing a matrix of conductive polymer device.

Regarding claim 61, Yoneda discloses second array of conductive channel (5a, 5b) comprises a metal coated channel [Col. 5, Lines 1-5].

Regarding claim 62, Chu discloses the third array of terminals 16 are insulated from the second metal layer 12b by a second layer of insulating mater1al 14b [Col. 5, Lines 3-11, Figures 1 and 3a].

With respect to claim 43, the claim is a method counterpart of structure of the rejected claims 62, 63 and 64 and method steps therefore are inherent for manufacturing a matrix of conductive polymer device.

Regarding claim 63, Yoneda discloses the second layer of insulating material 3b substantially covers second layer of metal 2b [Col. 4, Lines 31-40, Figure 1].

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Regarding claim 64, Chu discloses the fourth array of terminals 18 are electrically connected to the second metal layer 12b by interconnects 15 formed through second layer of insulating material 14b [Col. 5, Lines 3-11, Figures 1 and 3a].

Regarding claim 65, Chu discloses each of the array of second conductive channels 15 (for A and B) is provided at an end of each device of the matrix [see Figure 3a].

Regarding claim 66, Chu discloses each of the array of first conductive channels 13 and second conductive channels 15 are provided on opposing ends of each device (A and B) of the matrix [see Figure 3a].

With respect to claim 49, the claim is a method counterpart of structure of the rejected claim 66 and method steps therefore are inherent for manufacturing a matrix of conductive polymer device.

Regarding claim 70, Chu discloses at least one layer of device material comprises alternating layers of device material and layers of metal (12a, 12b)[Col. 4, Lines 31-41, Figure 1] and [Col. 5, Lines 32-38, Figure 3a].

With respect to claim 47, the claim is a method counterpart of structure of the rejected claim 70 and method steps therefore are inherent for manufacturing a matrix of conductive polymer device.

Regarding claim 71, Chu discloses the device is a PTC device and the device material is a PTC material [Col. 5, Lines 32-45, Figure 3a].

With respect to claim 48, the claim is a method counterpart of structure of the rejected claims 71 and method steps therefore are inherent for manufacturing a matrix of conductive polymer device.

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Response to Argument

Applicant's arguments with respect to claims 16-28, 32, 33, 43, 47-49, 54-66, 70, 71 and 73-76 have been considered but are moot in view of the new ground(s) of rejection.

Yoneda discloses a conductive channel which passes through and is insulated from the first metal layer and the layer of device material and a conductive element (conductive material) that connects the conductive channel to the second metal layer, whereby the first terminal is electrically connected to the layer of device material only through the first metal laye, and the second terminal is electrically connected to the layer of device only through the second metal layer.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, THIS ACTION IS MADE FINAL. See MPEP § 706.07(a).

Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joselito Baisa whose telephone number is (571) 272-7132. The examiner can normally be reached on M-F 5:30 am to 2:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Elvin Enad can be reached on (571) 272-1990. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Elvin G Enad/ Supervisory Patent Examiner, Art Unit 2832 Joselito Baisa Examiner Art Unit 2832

/J. B./

Examiner, Art Unit 2832